**8 BIT BOOTH MULTIPLIER**

A MINOR PROJECT REPORT

FOR

DIGITAL SYSTEM DESIGN FOR HARDWARE DESCRIPTION LANGUAGE

Submitted by:

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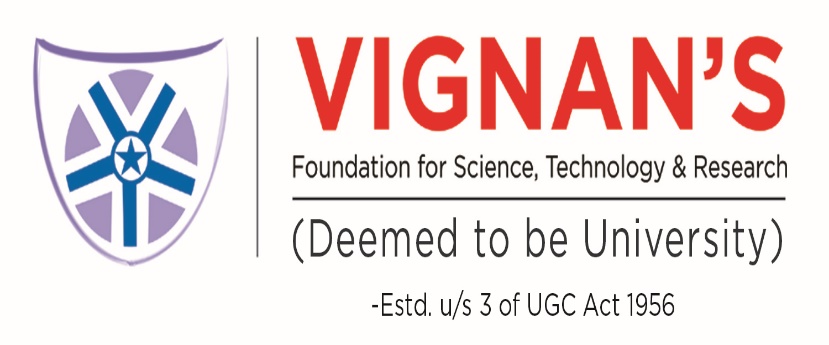
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IN

ELECTRONICS AND COMMUNICATION ENGINEERING

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DEPARTMENT OF

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**CERTIFICATE**

This is to certify that the minor project report entitled “**8-bit Booth Multiplier**” that is being submitted by M. Sai Kishore (171FA05305)

R.V.L.Karthik(171FA05329) & Tushar Chakravarthi(171FA05362) respectively in partial fulfilment for the award of II year II semester B.Tech degree in Electronics and Communication Engineering to Vignan’s Foundation for Science Technology and Research , is a record of work carried out by him/her under the guidance of Mr.D.Rajendra sir of ECE Department.

Signature of faculty guide Signature of department head

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**ABSTRACT**

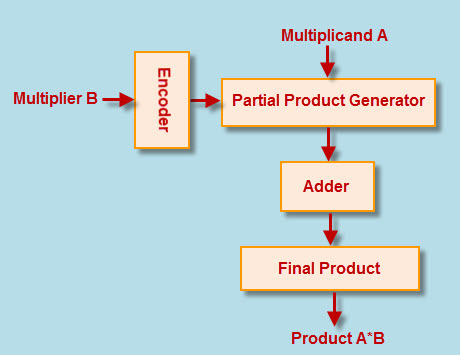
This project is about designing a 8-bit Booth Multiplier in Verilog and test its working by a test bench. The name 8-bit Booth multiplier itself tells that it uses the Booth’s algorithm to multiply the two numbers. Here we multiply two signed binary numbers. The first of those two numbers is the multiplicand and the second is the multiplier. The result that we get is the product. **Booth's algorithm** is of interest in the study of computer architecture.

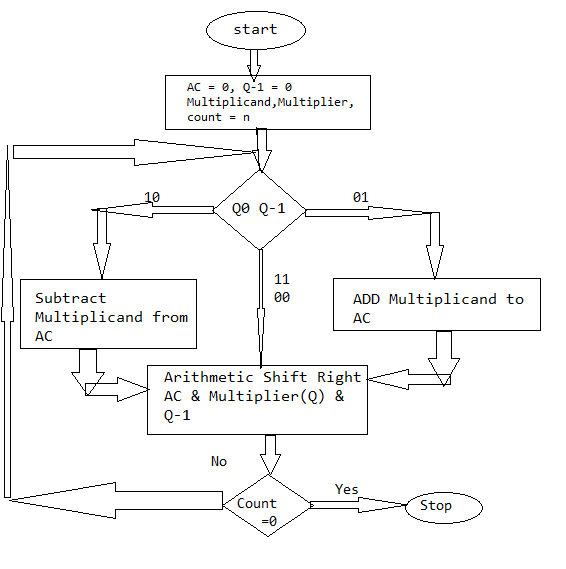
**INTRODUCTION**

Booth’s Multiplication Algorithm is a Multiplication algorithm that multiplies two signed binary numbers in two’s complement notation. The algorithm was invented by Andrew Donald Booth in 1950 while doing research on crystallography at Birkbeck college in Bloomsbury, London.

Booth’s algorithm for 8-bit binary numbers is also called a radix 8 Booth’s algorithm .Here we multiply two binary numbers each having 8 bits .The output product hence consists of 16 bit binary number.

**BLOCK DIAGRAM**

**FLOW CHART**



**VERILOG CODE**

* module multipiler(prod, busy, mc, mp, clk, start);
* output [15:0] prod;
* output busy;
* input [7:0] mc, mp;
* input clk, start;
* reg [7:0] A, Q, M;
* reg Q\_1;
* reg [3:0] count;
* wire [7:0] sum, difference;
* always @(posedge clk)
* begin
* if (start) begin
* A <= 8'b0;
* M <= mc;
* Q <= mp;
* Q\_1 <= 1'b0;
* count <= 4'b0;
* end
* else begin
* case ({Q[0], Q\_1})
* 2'b01 : {A, Q, Q\_1} <= {sum[7], sum, Q};
* 2'b10 : {A, Q, Q\_1} <= {difference[7], difference, Q};
* default: {A, Q, Q\_1} <= {A[7], A, Q};
* endcase
* count <= count + 1'b1;
* end
* end
* alu adder (sum, A, M, 1'b0);
* alu subtracter (difference, A, ~M, 1'b1);
* assign prod = {A, Q};
* assign busy = (count < 8);
* endmodule
* module alu(out,a,b,cin);
* output [7:0] out;
* input [7:0] a,b;
* input cin;
* assign out = a + b + cin;
* endmodule

**TEST BENCH**

* module testbench;
* reg clk, start;
* reg [7:0] a, b;
* wire [15:0] ab;
* wire busy;
* multipiler multipiler1(ab, busy, a, b, clk, start);
* initial begin
* clk = 0;
* $display("first example: a = 3 b = 17");
* a = 3; b = 17; start = 1; #50 start = 0;
* #80 $display("first example done");
* $display("second example: a = 7 b = 7");
* a = 7; b = 7; start = 1; #50 start = 0;
* #80 $display("second example done");
* $finish;
* end
* always #5 clk = !clk;
* always @(posedge clk) $strobe("ab: %d busy: %d at time=%t", ab, busy,
* $stime);
* endmodule

**ADVANTAGES**

1.Multiplication can be sped up.

2.When large number of consecutive 1s in multiplier replaces consecutive additions.

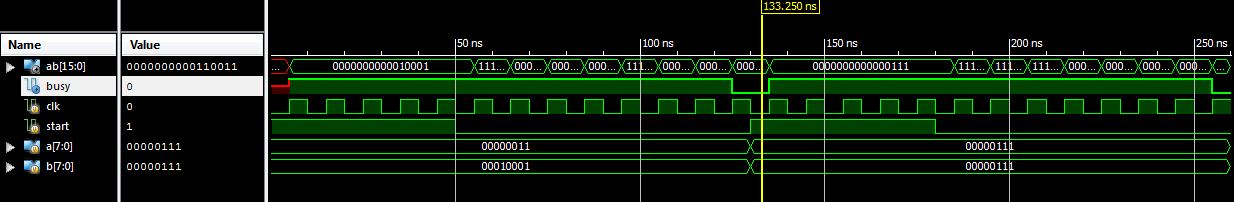
**DISADVANTAGES**

1.High power consumption.

**APPLICATIONS**

It used in ALU unit of computer to calculate multiplication of signed and unsigned number in binary form. This actually tells that how computer internally calculate signed  number multiplication.

**OUTPUT**

****

**CONCLUSION**

Hence 8-bit Booth Multipier is implemented and its function is verified using a test bench.